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Sensitivity analysis of transformerless PV inverter topologies to physical variations of power devices

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***Abstract*—Transformerless (TL) topologies are employed in 1ϕ PV inverter topologies due to their small size and low weight. Avoiding the grid side transformer requires the modulation technique and the basis topology to be accordingly changed in order to mitigate dc current components in the grid side and the leakage current to ground.**

This paper carries out a sensitivity analysis of selected TL topologies. This analysis investigates the impact of parameter variations of the employed semiconductor devices and detects the device which affects the most the overall efficiency. As a result, relevant info for engineers selecting the most suitable power devices for the implementation of a certain TL topology is provided.

***Index Terms*—Transformerless PV inverters, sensitivity analysis.**

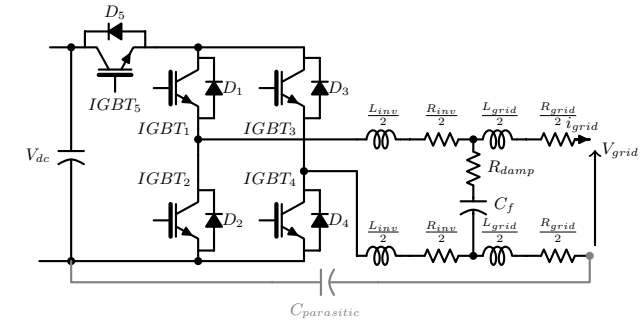
I. Introduction

As a result of the last decade's researching activity on PV inverters, a number of transformerless (TL) topologies for 1ϕ PV inverters has been developed in order to reduce the size and weight of the commercial equipments while increasing the overall efficiency. However, these topologies have some drawbacks, such as the injection of dc current components at the grid side and a higher number of power devices in comparison to the basic transformer-based topology (H4). The injection of dc currents at the grid side can be avoided by the employment of appropriate control techniques while a higher number of power devices is required in order to reduce leakage currents flowing through the parasitic capacitor of the PV generator by decoupling the grid during the freewheeling period of the inverter current. TL-based 1ϕ PV inverters are commercially available and manufacturers have developed their own inverter series based on transformerless topologies (H5, HERIC, HB-NPC and H6, respectively) [1].

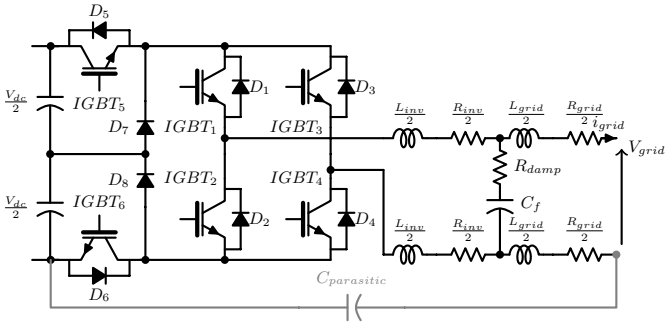
The performances of TL topologies have been analyzed in the literature considering diverse characteristics, i.e. efficiency and dc-current component, and standards applicable to grid connected PV inverters. This is the case in [2], where the leakage current of a H4 topology, without a grid-side transformer, is evaluated for diverse LCL filter configurations and modulation techniques. H5, HERIC, NPC and FB-ZVR topologies are analyzed and evaluated experimentally in [3]. [4] compares the performance of H5, HERIC, H6, FB-ZVR, HB-NPC and Araujo inverter by means of simulation tests in terms of the European Efficiency, output current THD and leakage current. The HERIC topology reaches a $\eta_{EU} = 98.27$ % while the lowest THD corresponds to H6 and no leakage current is obtained in case of NPC topologies. The behavior of H5, HERIC and H6 topologies is analyzed and compared in terms of power losses in [5], where the proposed H6 topology shows a lower efficiency than HERIC but higher than H5 (the measured European Efficiencies in 1 kW prototypes for H5, HERIC and H6 are 96.78 %, 97 % and 97.09 %) and the minimum leakage current corresponds to H5 (6 mA). Neutral Point Clamped converters are analyzed in [6], where it is shown that the European Efficiency reaches 96.4 %, 96.9 %, and 97.2 % for FB-DCBP, oH5 and PN-NPC topologies, respectively. In [7] the losses of a 1 kW prototype are compared by means of simulation tests for H5, oH5, H6, HERIC, HBZVR and HBZVR-D and the leakage currents are measured experimentally. The obtained results show that HERIC topology results in a higher efficiency (96.05 %) and the lowest leakage current corresponds to HBZVR-D (42.7 mA). Similar analyses have been carried out in [8] and [9] and, in all cases, the obtained results, both in simulation and experimentally, are valid for the case of the power devices selected for simulation purposes or the implementation of prototypes.

A statistical approach for performance evaluation of PV inverters is proposed in [10] and applied to a transformer-based H4 topology. The variability of IGBT and diode parameters due to the employed technology and the characteristics of the manufacturing process allows the performance of PV inverter topologies to be evaluated during the design stage. This work applies this statistical approach in order to evaluate four TL topologies (H5, H6, HB-NPC and HERIC) and determine the switch whose characteristics affect the most the overall performance: PV inverter efficiency, dc-component of the grid-side current and leakage current.

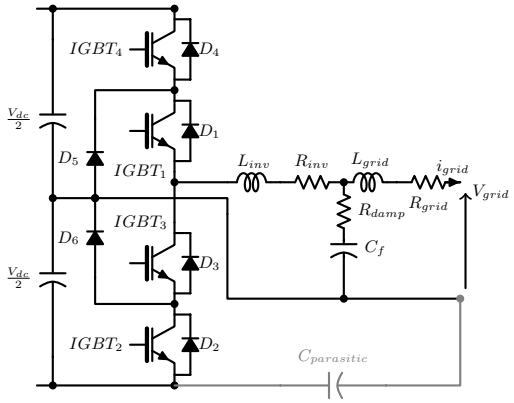
The evaluated topologies are described in Section II. The procedure applied to carry out the sensitivity analysis is given in Section III. Section IV provides the obtained simulation results and, finally, Section V provides the conclusions of this work.



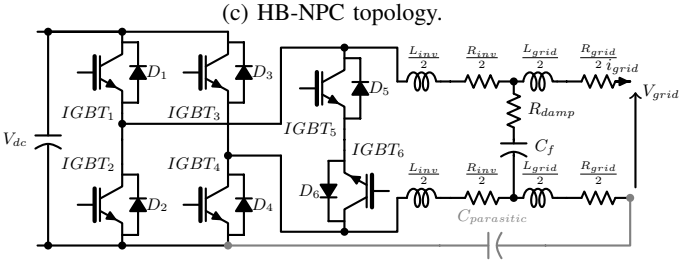
(a) H5 topology.



(b) H6 topology.



(c) HB-NPC topology.



(d) HERIC topology.

Fig. 1: Evaluated transformerless topologies.

II. Evaluated TL topologies

A. H5

The H5 topology consists of a full-bridge with one additional switch in the DC-link as shown in Fig. 1.a which enables the decoupling of the PV inverter from the grid during the freewheeling period of the current [4]. The switches #1 ($IGBT_1$+D_1) and #3 ($IGBT_3$+D_3) in the top half of the full-bridge are switched with grid frequency, switches #2 ($IGBT_2$+D_2), #4 ($IGBT_4$+D_4), and #5 ($IGBT_5$+D_5) are operated at high frequency. For creating a positive output voltage #1 is continuously switched on during the positive half wave and #4 and #5 are switched simultaneously. Thus, the current flows through #5, #1, and returns through #4. For obtaining the zero voltage vector #4 and #5 are turned off. During this freewheeling period the current flows through #1 and the anti-parallel diode of #3. The negative voltage output is similarly achieved by the switches #2, #3, and #5.

The current contains a switching ripple which is equal to the switching frequency resulting in high filtering effort. However, due to the fact that the voltage across the filter is unipolar, low core losses can be expected. Another advantage of the H5 topology can be found in the low leakage current. This is because the voltage to ground V_{PE} is sinusoidal with grid frequency component.

B. H6

The H6 topology, also known as Full-Bridge Inverter with DC Bypass (FB-DCBP), is shown in Fig. 1.b. This topology consists of a full-bridge with two extra switches, #5 ($IGBT_5$+D_5) and #6 ($IGBT_6$+D_6), in the DC-link and two clamping diodes (D_7 and D_8) which are connected at the midpoint of the DC-link capacitance [1]. #5 and #6 separate the PV panels from the grid during the zero voltage states while D_7 and D_8 ensure that the zero voltage is grounded. The full-bridge is operated at the grid frequency (#1 and #4 are switched on for positive output voltages and #2 and #3 for negative) and #5 and #6 are switched at high frequency for generation of the active voltage vector.

As in the case of H5, the voltage across the output filter is unipolar and V_{PE} has only a grid frequency component, resulting in low core losses and a low leakage current, respectively.

C. HB-NPC

In contrast to H5 and H6 the HB-NPC topology (*Half Bridge - Neutral Point Clamped*) is not based on the full bridge concept. As it can be seen in Fig. 1.c the HB-NPC is a half-bridge consisting of the four switches #1 to #4 and the two clamping diodes D_5 and D_6 which are connected to the neutral grid terminal at the midpoint of the DC-link capacitance [4]. The diodes limit the voltage which is applied to the switches to half of the PV input voltage. This means that the NPC requires twice the PV input voltage in comparison to full-bridge topologies [1]. #1 and #3 are switched with grid frequency, #2 and #4 are operated at high frequency. In order to create a positive output voltage, #4 is switched while #1 is continuously turned on during the positive half wave. With #4 switched off the zero voltage state is created. The current flows through D_5 and #1 in the freewheeling period. For achieving

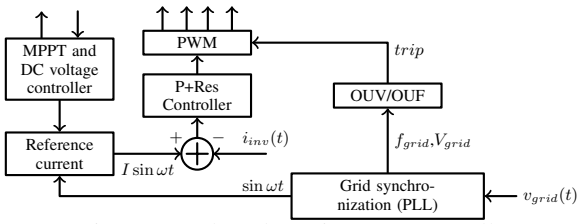


Fig. 2: Employed PV inverter controller.

a negative output voltage, #2 and #3 are switched in a similar manner.

In case of the NPC the current also contains a switching ripple which is equal to the switching frequency resulting in high filtering effort, but here again the core losses are low due to an unipolar voltage across the filter. One remarkable advantage of this topology is that V_{PE} is constantly equal to $-\frac{V_{in}}{2}$ which means that no leakage current is obtained [4].

D. HERIC

Based on a full-bridge the HERIC topology (*Highly Efficient and Reliable Inverter Concept*) contains an additional bi-directional switch on the AC side for decoupling the PV inverter from the grid during the freewheeling periods [4]. The topology is shown in Fig. 1.d. As shown, the bidirectional switch is built up of two switches, $IGBT_5$ and $IGBT_6$, plus their anti-parallel diodes D_5 and D_6 (#5 and #6, respectively). #5 and #6 are switched at grid frequency, #1 to #4 are operated at high frequency. During the positive half wave #5 is turned on and #1 and #4 are switched simultaneously in order to obtain a positive output voltage. The corresponding zero voltage state is achieved by turning off #1 and #4, so that the current flows through $IGBT_5$ and D_6 on the AC side only. For creating the negative voltage vector #6 is continuously turned on during the negative half wave and #2 and #3 are switched concurrently.

Similar to the H5 topology high filtering effort is also needed for the HERIC topology due to the fact that the current contains a switching ripple equal to the switching frequency. Nevertheless, low core losses are obtained by the unipolar voltage across the filter and a low leakage current is achieved due to a sinusoidal V_{PE}.

III. Simulation Model

The transfomerless topologies described in the previous section have been evaluated by means of simulation tests in order to determine the power device which affects the most the overall performance, and the way this performance is changed, considering the physical characteristics of the commercially available power devices.

The employed controller has the same general structure in all the cases and only the PWM block changes, according to the analyzed topology. The general structure of this controller is shown in Fig. 2. The reference current $I \sin \omega t$ depends on the available power of the PV system, which will change the amplitude I, and the synchronization signal provided by a Phase Locked Loop (PLL) applied to the grid voltage (v_{grid}). The PLL measures both the amplitude and the frequency of the electrical grid in order to trip the inverter if OUV/OUF condition arises. The reference current for injection purposes is compared to the measured one in order to generate the error signal applied to the current controller, which is implemented by means of a Proportional-Resonant controller [1]. The other simulation parameters are shown in Table I. As it can be seen, no further optimizations for each topology have been carried out in order to compare the topologies under the same LCL filter parameters. In the case of the HB-NPC topology the main issue is the uneven distribution of the switching losses. This means that by optimizing the switching frequency the losses are reduced and the overall efficiency increases. It has been reported in [11] that the outer switches (here #2 and #4) are stressed more due to the switching losses than the inner switches which operate at grid frequency and that the uneven losses distribution increases with increasing switching frequency. Thus, the optimization of the switching frequency of the HB-NPC topology at fixed LCL parameters, which allows the reduction of the switching frequency in comparison to the other topologies, would lead to lower switching losses of the outer switches and thus to an increasing efficiency. However, the aim of this work is not comparing PV converter topologies in terms of absolute efficiency, but investigating the impact of practical devices' characteristics on the overall converter performance and, hence, absolute efficiency values are not relevant.

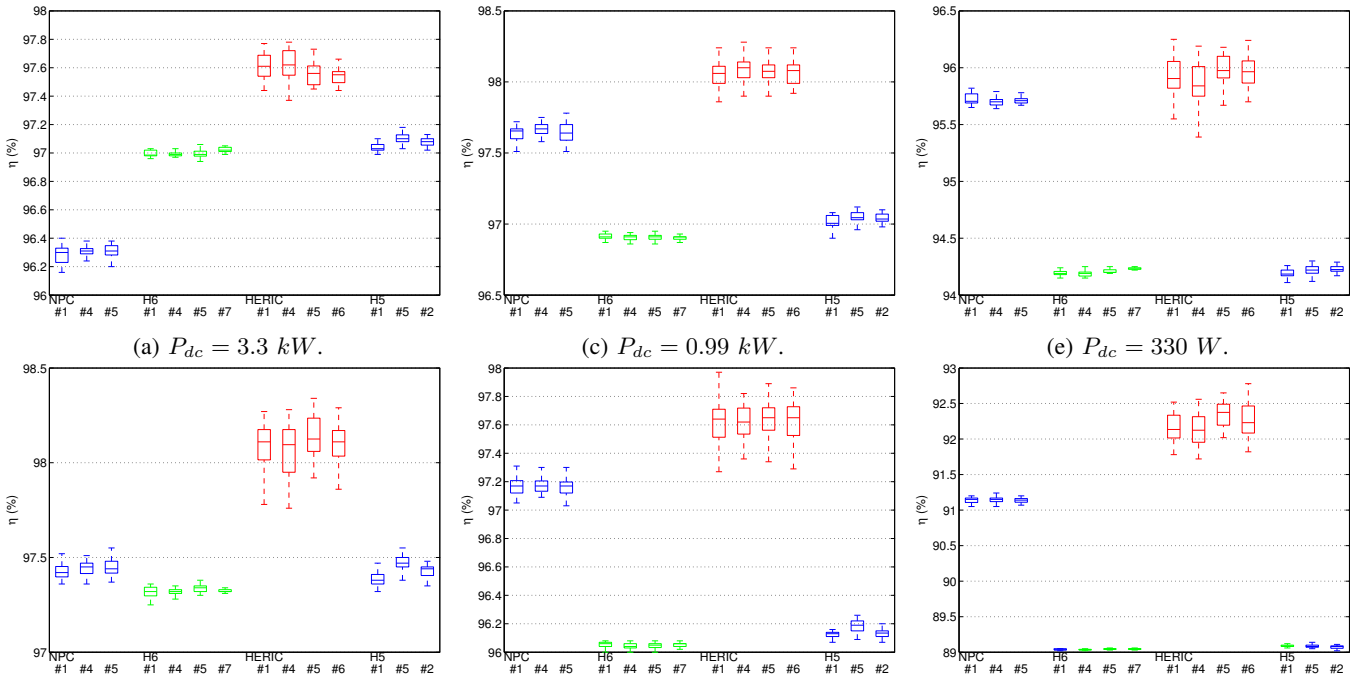
TABLE I: Simulation Parameters.

Parameter	Value
L_{inv}	4.7 mH
R_{inv}	0.2 Ω
L_{grid}	2.1 mH
R_{grid}	0.1 Ω
C_f	10 μF
R_{damp}	10 Ω
$C_{parasitic}$	100 nF
P_n	3.3 kW
V_{grid}	230 V^{rms}
f_{grid}	50 Hz
f_{sw}	6 kHz
V_{dc}	600 V

A. Sensitivity analysis of TL topologies

In order to determine the switch which affects the most the performance of each TL topology, a set of switches for each topology has been selected and a full set of simulation tests has been carried out for each switch. The comparison of the obtained results allow the most sensitive switch to be determined considering that the employed switches are practically implemented by means of real power devices subjected to certain variations according to the manufacturer specifications, given in the datasheets.

Due to the symmetrical behavior of the topologies for both the positive and negative output voltages only half of the required power devices have been considered. Table II shows the selected switches for the sensitivity analysis. For



(a) $P_{dc} = 3.3\ kW$. (c) $P_{dc} = 0.99\ kW$. (e) $P_{dc} = 330\ W$.

(b) $P_{dc} = 1.65\ kW$. (d) $P_{dc} = 660\ W$. (f) $P_{dc} = 165\ W$.

Fig. 3: Probability distributions of efficiencies at each tested power level. Most and least robust topologies are ploted in green and red boxes respectively.

TABLE II: Selected switches for the sensitivity analysis.

Topology	Switches
H5	#1, #2 and #5
H6	#1, #4, #5 and #7
HB-NPC	#1, #4 and #5
HERIC	#1, #4, #5 and #6

the evaluation of the sensitivity to each selected switch Monte Carlo (MC) tests have been carried out by changing the switch parameters, i.e. conduction resistance and stray inductance, according to the limits established for the available commercial power devices. The parameters corresponding to other power devices in each topology have been established considering the mean values. The probability distribution functions employed to determine the limits and mean values for 12 IGBT and diode parameters have been provided in [10].

In order to reduce the computational burden associated to MC tests, Latin Hypercube Sampling (LHS) has been applied to generate the parameters of the analyzed switch. As a result, 30 sets of 12 parameters for each analyzed switch, within the limits provided by the probability distribution functions in [10] and accordingly weighted by LHS, have been generated for simulation purposes.

IV. Simulation Results

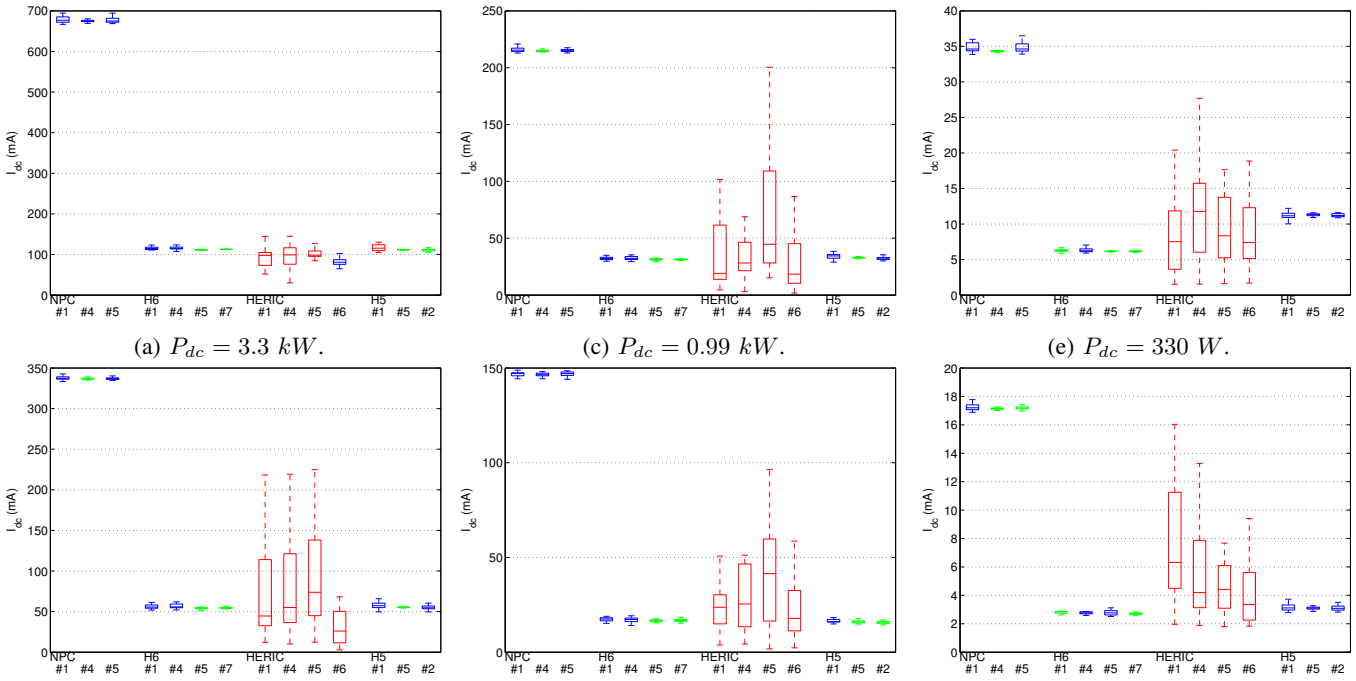
The evaluation of the selected transformerless topologies has been carried out considering the efficiency at each power level (100%, 50%, 30%, 20%, 10% and 5% of the nominal power), the European Efficiency, the DC component of the grid side current and the leakage current. The simulations have been carried out by means of MATLAB/Simulink and PLECS. According to the procedure described in the previous section, the following results are given as probability distribution functions (pdfs).

A. *Efficiency vs Power*

The efficiency of each TL topology has been evaluated for each selected switch and considering the set of parameters which matches the available commercial components. The results of these tests are shown in Fig. 3. The topology resulting in the highest mean efficiency at each power level is HERIC but, as it can be seen, it also results in the greatest variability. The topology with the lowest variability is H6 and, as a consequence, this topology exhibits the highest robustness to the variability of the power devices' parameters with respect to the applied testing conditions. Considering the sensitivity analysis, H5 and HERIC show the greatest changes in the efficiency when changing from one to another of the selected devices. HB-NPC and H6 provide almost the same efficiency for all the analyzed switches. As a consequence, the efficiency of HB-NPC and H6 at each power level depend less on the characteristics of the employed power devices than in the case of H5 and HERIC.

B. *Grid-side dc current component*

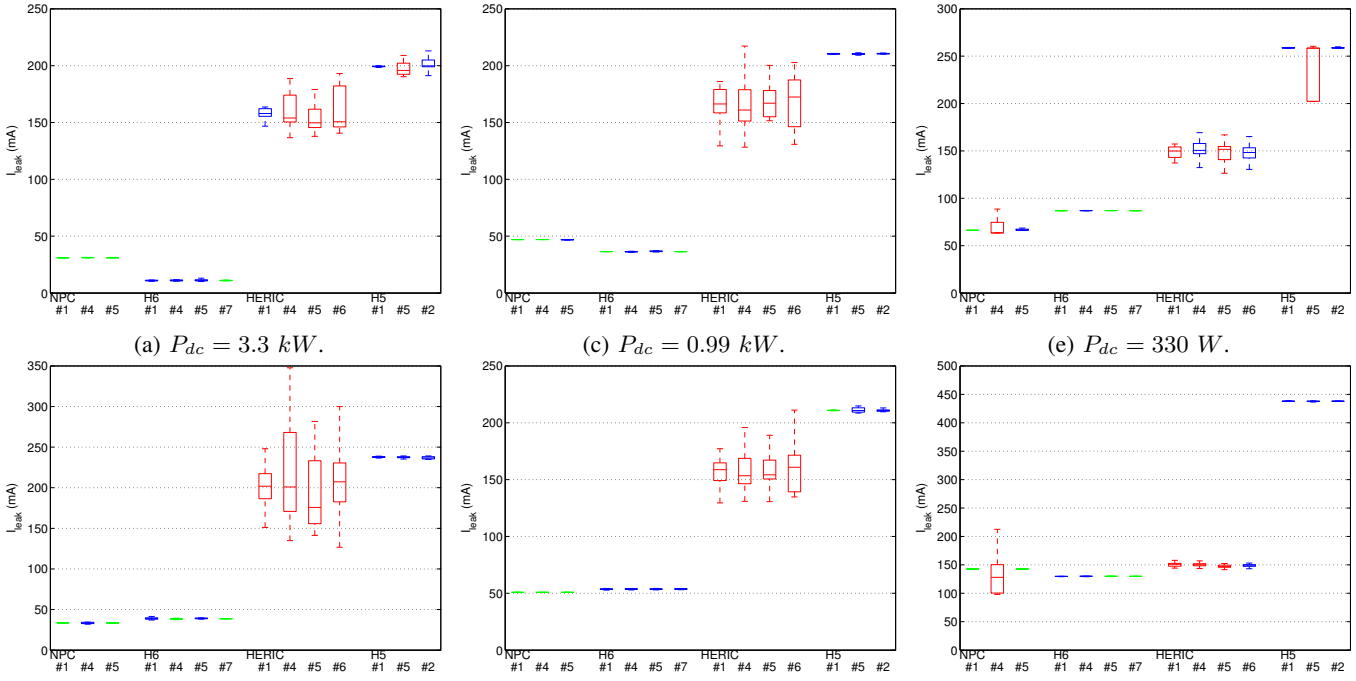
Fig. 4 shows the evolution of the dc current component at the grid-side depending on both the analyzed power level and the switch. As can be seen, in all the analyzed cases,



(a) $P_{dc} = 3.3\ kW$. (c) $P_{dc} = 0.99\ kW$. (e) $P_{dc} = 330\ W$.

(b) $P_{dc} = 1.65\ kW$. (d) $P_{dc} = 660\ W$. (f) $P_{dc} = 165\ W$.

Fig. 4: Probability distributions of dc current components at the grid side. Most and least robust topologies are ploted in green and red boxes respectively.

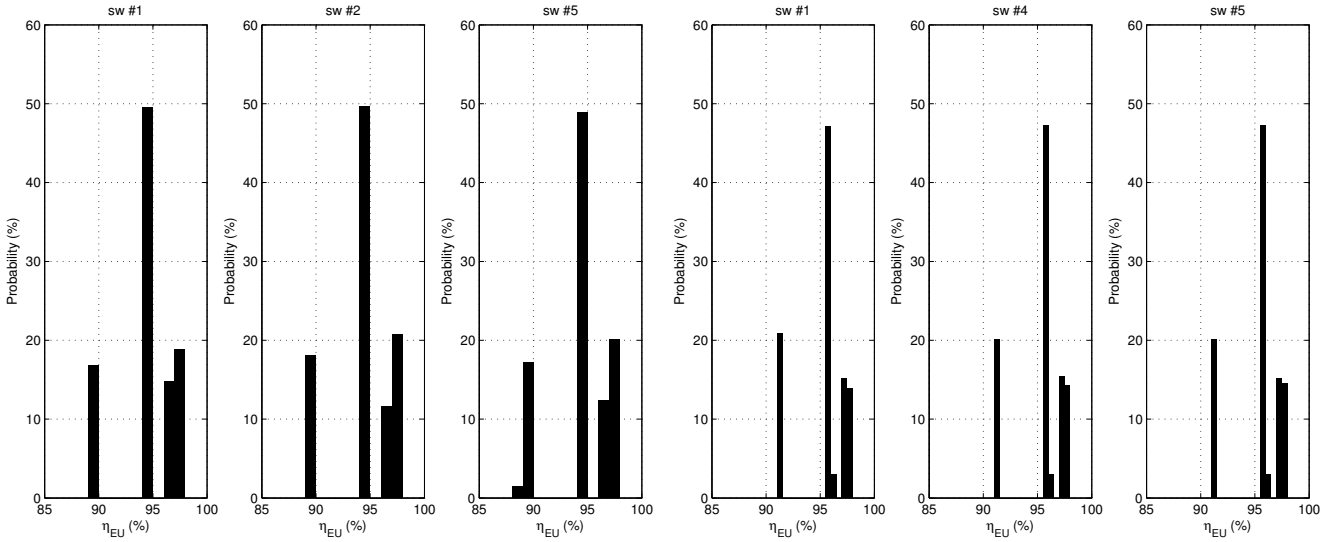


(a) $P_{dc} = 3.3\ kW$. (c) $P_{dc} = 0.99\ kW$. (e) $P_{dc} = 330\ W$.

(b) $P_{dc} = 1.65\ kW$. (d) $P_{dc} = 660\ W$. (f) $P_{dc} = 165\ W$.

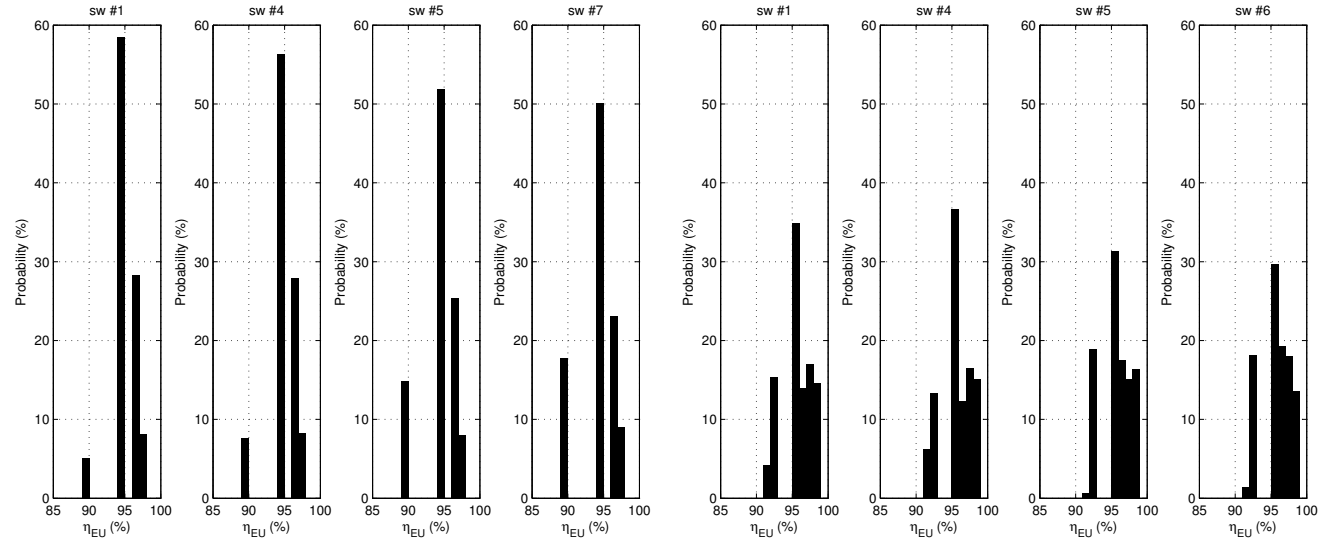
Fig. 5: Probability distributions of peak leakage currents. Most and least robust topologies are ploted in green and red boxes respectively.

the mean value of the dc current component decreases when reducing the PV inverter power. The worst mean dc current is obtained in case of the HB-NPC topology at the nominal power, reaching $0.68\ A$. As counterpart, this value is almost maintained for the three analyzed switches (the maximum variation is $3\ mA$ at all the analyzed power levels). H5 and H6 results on equivalent performances, with a maximum dc current around $115\ mA$ and, as in the previous case, switches



(a) H5. #1: $\mu = 94.52$ % and $\sigma = 2.55$ %, #2: $\mu = 94.45$ % and $\sigma = 2.61$ %, #5: $\mu = 94.41$ % and $\sigma = 2.66$ %.

(c) HB-NPC. #1: $\mu = 95.33$ % and $\sigma = 2.23$ %, #4: $\mu = 95.37$ % and $\sigma = 2.2$ %, #5: $\mu = 95.37$ % and $\sigma = 2.21$ %.



(b) H6. #1: $\mu = 95.05$ % and $\sigma = 1.68$ %, #4: $\mu = 94.92$ % and $\sigma = 1.89$ %, #5: $\mu = 94.51$ % and $\sigma = 2.33$ %, #7: $\mu = 94.35$ % and $\sigma = 2.48$ %.

(d) HERIC. #1: $\mu = 95.79$ % and $\sigma = 2.02$ %, #4: $\mu = 95.76$ % and $\sigma = 2.07$ %, #5: $\mu = 95.88$ % and $\sigma = 1.98$ %, #6: $\mu = 95.86$ %, $\sigma = 1.97$ %.

Fig. 6: Probability distributions of the European Efficiency for the tested topologies and the selected switches.

variations have almost no impact on the measured values (the maximum variation between switches is 5 mA). The HERIC topology, while resulting on the lowest mean dc-current (99 mA), exhibits the greatest sensitivity to changes in parameters (Fig. 4.b), showing widely spread pdfs. Moreover, depending on the switch under analysis, the mean value of the dc-current can change a lot, resulting in the highest and least average currents for #5 and #6 respectively.

C. Leakage current

Fig. 5 shows the obtained peak leakage currents. As can be seen, the leakage current increases with lower power levels in HB-NPC and H6. In H5 and HERIC the mean value of the leakage current is almost maintained in 3 power levels. The worst value corresponds to H5, at the lowest power level, reaching 0.44 A. The best performances correspond to H6 and HB-NPC at the nominal power, reaching 11 mA and 31 mA respectively. In the case of HB-NPC, the switch resulting in the lowest peak leakage current is #4 but its corresponding pdf spreads widely, affecting the most the equipment characteristics. For H5 and H6, almost all the switches perform the same but, for H5 variations of #5 at 3.3 kW, 660 W and 330 W result in spread pdfs. The pdfs of the peak leakage current for HERIC are very widespread and the device which results in lower peak leakage currents at higher power levels (3.3 kW and 1.65 kW) is #5.

D. European Efficiency

The pdfs in Fig. 3 have been employed, according to

$$\begin{aligned}\eta_{EU} = \quad & 0.03 \cdot \eta_{5\%} + 0.06 \cdot \eta_{10\%} + 0.13 \cdot \eta_{20\%} \\ & +0.1 \cdot \eta_{30\%} + 0.48 \cdot \eta_{50\%} + 0.2 \cdot \eta_{100\%}\end{aligned} \quad (1)$$

to generate the probability distribution functions of the EU efficiency, shown in Fig. 6. As can be seen, HERIC is the topology which achieves the highest EU efficiency (a mean value of $\eta_{EU} = 95.88$ % for switch #5) and the lowest EU efficiency is obtained in case of H6 (a mean value of $\eta_{EU} = 94.35$ % for the clamping diode $Drr7$). From the point of view of the sensitivity, HB-NPC provides almost the same performance for each tested switch, reaching $\eta_{EU} = 95.33$ %, $\eta_{EU} = 95.37$ % and $\eta_{EU} = 95.37$ % for switches #1, #4 and $Drr5$ respectively. H6 exhibits the greatest changes of the EU efficiency, from $\eta_{EU} = 94.35$ % for the clamping diode $Drr7$ to $\eta_{EU} = 95.05$ % for switch #1. In the case of H5, the worst results in terms of EU efficiency are obtained for switch #5, which results in an average efficiency $\eta_{EU} = 94.41$ %. As a consequence, HB-NPC is the less sensitive topology to switches' characteristics mismatches and H6 is the most sensitive one.

As a result of the employed statistical approach for sensitivity evaluation, the pdfs provide information on the most probable value and the standard deviation (σ). These values are relevant for PV inverter manufacturers in order to evaluate the quality of the developed equipment. From Fig. 6, it can be seen that the HB-NPC shows almost the same pdf for each analyzed switch, resulting in $\sigma = 2.2$ %. The most probable EU efficiency, at $\eta_{EU} = 95.75$ %, is maintained at 47.2 % for the three analyzed switches. The standard deviations for HERIC change a bit more, from $\sigma = 1.97$ % for switch #6 to $\sigma = 2.07$ % for switch #4. EU efficiencies of up to 98.5 % can be reached (with probabilities around 16.4 %) but the most probable value at $\eta_{EU} = 95.5$ % moves from 36.6 % to 29.6 %. In the case of H5, the values of the standard deviation change from $\sigma = 2.55$ % to $\sigma = 2.66$ %, with the most probable EU efficiency at $\eta_{EU} = 94.5$ % at a probability that ranges from 49.5 % to 48.9 % for switches #1 and #5, respectively. Finally, the H6 topology shows the highest probability for the most probable EU efficiency by reaching a 58.5 % probability of having $\eta_{EU} = 94.5$ %. However, with a range from 1.68 % to 2.48 % the standard deviation changes the most in this case.

V. Conclusion

This work evaluates the sensitivity of H5, H6, HERIC and HB-NPC topologies in 1ϕ PV inverters to parameter changes in IGBTs and diodes, which result from the manufacturing process of power devices and the employed technology. The simulation results show that, considering the European Efficiency and comparing the obtained pdfs for each tested switch, HB-NPC and H6 are the least and most sensitive topologies respectively, with clamping diodes in H6 having the biggest impact on its performance. However, H6 exhibits the lowest mean variability of its performance ($\sigma = 1.68$ % for #1) while σ changes the most across the developed tests (from $\sigma = 1.68$ % to $\sigma = 2.48$ % for #1 and #7 respectively). In the case of dc current injection, HERIC shows the lowest value at nominal power but the obtained pdfs are widespread and its behavior changes a lot depending on the real parameters of its switch. The lowest dc currents at each power level are obtained in case of variations of parameters associated to the ac side diodes. In the case of the leakage current, H6 performs better, having the same results at each power level for all the switches.

The applied analysis is based on a statistical approach which allows the probability distribution function of the selected performance indicators (European Efficiency, grid-side dc-current component and peak leakage current) to be obtained. The poposed evaluation method can be applied during the design stage in order to select the most suitable power devices for the implementation of each topology switch.

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